WHAT IS CLAIMED IS:

1. An adaptive phase controller employing a threshold level, comprising:

a comparator configured to receive a comparison signal representing a phase and to provide a vernier signal based on comparing first and second samples of said comparison signal when said comparison signal is below said threshold level; and

an adder/decoder coupled to said comparator and configured to adjust a current number corresponding to said phase based on said vernier signal.

2. The adaptive phase controller as recited in Claim 1 wherein said adder/decoder is configured to increment said current number when said first sample is greater than said second sample.

3. The adaptive phase controller as recited in Claim 1 wherein said adder/decoder is configured to decrement said current number when said first sample is less than said second sample.

4. The adaptive phase controller as recited in Claim 1 wherein said adder/decoder is configured to maintain said current number when said first sample is equal to said second sample.

5. The adaptive phase controller as recited in Claim 1 further comprising a comparator configured to provide a reset signal when said comparison signal reaches said threshold level.

6. The adaptive phase controller as recited in Claim 5 further comprising an adder/decoder configured to reset a current number to a reset number employing said reset signal.

7. The adaptive phase controller as recited in Claim 6 wherein said reset number is determined empirically.

8. A method of controlling a phase employing a threshold level, comprising:

receiving a comparison signal;

providing a vernier signal based on comparing first and second samples of said comparison signal when said comparison signal is below said threshold level; and

adjusting a current number corresponding to said phase based on said vernier signal.

9. The method as recited in Claim 8 wherein said adjusting includes incrementing said current number when said first sample is greater than said second sample.

10. The method as recited in Claim 8 wherein said adjusting includes decrementing said current number when said first sample is less than said second sample.

11. The method as recited in Claim 8 wherein said adjusting includes maintaining said current number when said first sample is equal to said second sample.

12. The method as recited in Claim 8 wherein said providing further includes providing a reset signal when said comparison signal reaches said threshold level.

13. The method as recited in Claim 12 wherein said adjusting further includes resetting a current number to a reset number employing said reset signal.

14. The method as recited in Claim 13 wherein said reset number is determined empirically.

15. A transmitter, comprising:

an input section that receives in-phase and quadrature phase input and feedback signals and provides in-phase and quadrature phase output signals;

a feedback section that provides in-phase and quadrature phase feedback signals to said input section;

a power amplifier that employs said input and feedback sections;

a local oscillator section that is coupled to said feedback section;

a digitally controlled phase shifter that is coupled to said input and local oscillator sections; and

an adaptive phase controller that employs a threshold level and is coupled to said digitally controlled phase shifter, including:

a comparator that receives a comparison signal representing a phase between said input and output signals and provides a vernier signal based on comparing first and second samples of said comparison signal when said comparison signal is below said threshold level; and

an adder/decoder, coupled to said comparator, that adjusts a current number corresponding to said phase based on said vernier signal.

16. The transmitter as recited in Claim 15 wherein said adder/decoder increments said current number when said first sample is greater than said second sample.

17. The transmitter as recited in Claim 15 wherein said adder/decoder decrements said current number when said first sample is less than said second sample.

18. The transmitter as recited in Claim 15 wherein said adder/decoder maintains said current number when said first sample is equal to said second sample.

19. The transmitter as recited in Claim 15 further comprising a comparator that provides a reset signal when said comparison signal reaches said threshold level.

20. The transmitter as recited in Claim 19 further comprising an adder/decoder that resets a current number to a reset number employing said reset signal.

21. The transmitter as recited in Claim 20 wherein said reset number is determined empirically.